100G UDPIP Hardware Protocol Stack Core

The core Implements a UDP/IP hardware protocol stack that enables high-speed communication over a LAN or a point-to-point connection. It is ideal to offload systems from demanding tasks of UDP/IP and to enable media streaming in both FPGA and RISC designs.

The core supports ARP request, reply and manages 32-entry ARP cache. ICMP ping reply is included. The core provides DHCP client engine, which can get an IP address from external DHCP servers. The 100G UDPIP Core implements V3 IGMP membership Query/Report messaging. The IP jumbo packets are supported as well as UDP port number filters and VLAN.

IP/UDP checksum generation and validation are implemented. MDIO bus access to external device via AXI4-Lite bus is included. IP raw packets are supported in both TX and RX.

IP fragmentation and TCP hardware protocol stack companion core are available on demand.

The core supports 32 RX channels and 32 TX channels. Each of the RX channels can be configured and associated with any of five RX ports. Each of the TX channels can be used to send IP packets on any of five TX Ports.

The core connects to user logic through Control Interface of AXI4-Lite buses; five RX Dedicated Ports of AXI4-Stream buses and five TX Dedicated Ports of AXI4-Stream buses.

The core connects to 100G MAC module through AXI4-Stream bus. KMX 100G MAC and PCS cores are available to our customers.

The core is designed to well handle exceptions of internal memory exhaustion and invalid incoming packets while it makes the max use of internal memory to deal with RX and TX burst traffic effectively.

There is a fully implemented reference design with KMX 100G UDPIP core whose VHDL source code is shipped with the core delivery.

Features

Full 100G UDP/IP Hardware Stack Core

- 100G Ethernet
- IPv4
- Transmit and Receive
- Five RX ports with 32 RX channels and Five TX ports with 32 TX channels
- ARP client/server with 32 entry ARP table
- ICMP (Ping Reply)
- IGMP v3 membership Query/Report messaging
- Multicast
- UDP Port Filtering
- 801.1Q tagging for VLAN
- UDP/IP Checksum generation and validation
- DHCP client engine
- TCP hardware protocol stack companion core available on demand
- IP raw packets
- Run time programmable network parameters
- Control/Status interface
- Separate clock domains for packet processing and control interfaces.
- IP Fragmentation available on demand
- MAC, PCS, MDIO modules
- External MDIO access via AXI4-Lite bus

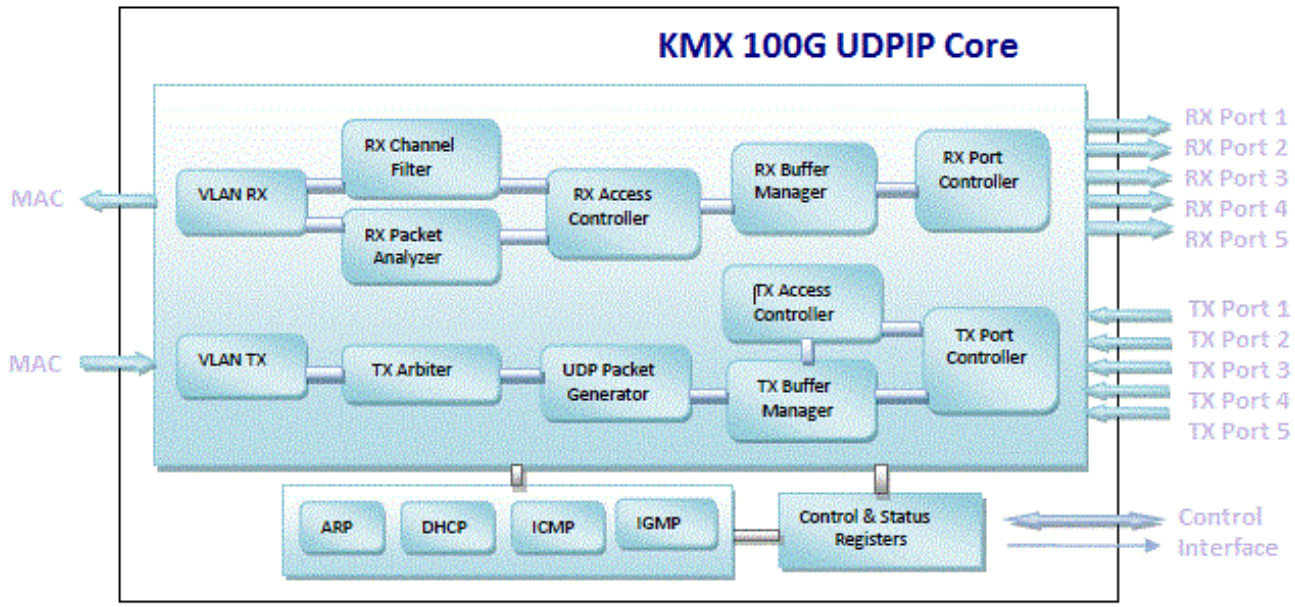

Figure 1 KMX 100G UDP/IP Core Architecture

Applications

The core is widely used in applications where ultra-low, deterministic latency and high performance of throughput are required, such as video, image and audio streaming over Ethernet, IP cameras VOIP and smart phones, high frequency trading system, high-speed communication data centers, device monitoring and control over IP networks.

Implementation Results

The 100G UDPIP Core has been evaluated on both Xilinx and Altera platforms. The core is highly pipelined and optimized to achieve ultra-low latency and high performance. The following list the core sample resource utilization on Xilinx Kintex UltraScale+ FPGA device KCU116 board.

Core Configuration	LUT	LUTRAM	BRAM	FF
5 RX Ports & 5 TX Ports	15277	936	44	12844

Support

The core as delivered is warranted against defects. Any update of the core and free technical support is provided 7 days a week and 24 hours a day to the customers with a valid KMX license.

Deliverables

The core in netlist format included, the delivery package contains everything required for successful integration, including VHDL source code of reference design and test bench, verification scripts, constrain file, synthesis scripts, and related documents. Free companion cores such as MDIO, serial debug command, auto-configuration are shipped with the core to help customers with easier and efficient integration.

Contact

Please contact KMX Embedded Core team, if you are interested in KMX 100G UDPIP core.

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