KMX EMBEDDED CORE 40G MAC and PCS Core

KMX 40G MAC and PCS core, which including media access control (MAC) module, physical coding sublayer (PCS) module and physical medium attachment (PMA) module, is compliant with the IEEE 802.3ba-2010 standard. The core supports RS FEC as defined in Clause 74 IEEE 802.3 with independent error bit detection and error bit correction.

KMX 40G MAC module connects to user logic via AXI4-Stream interface of 128 bits at 312.5MHZ and to 40G PCS core via XLGMII interface of 128 bits at 312.5 MHZ. It also connects to user logic via AXI4-Lite interface.

The MAC core accepts packets from user logic and generates new format packets by adding Preamble/SFD; padding zero bytes for short packets to 64 bytes; generating 32 bit CRC and padding it. It receives packets from 40G PCS via XLGMII interface and generates new format packet by removing Preamble/SFD and 32 bit CRC after CRC checking.

It supports Pause Frame processing for flow control and implements Deficit Idle Count algorithm to ensure maximum possible throughput at the transmit interface.

It implements internal XLGMII loopback for debug purpose, which at XLGMII interface, the data flow on TX path is redirected to RX path and no data is forwarded to the transceiver TX interface.

It implements configuration, control, status and statistical information collection, and it supports VLAN tagged frame defined IEEE 802.1Q.

KMX 40G PCS module connects to 40G MAC module via XLGMII of 128 bits at 312.5MHZ and connects to transceiver interface at 256 bits at 161.1328125MHZ. The PCS core is compliant with IEEE 802.3ba specifications. KMX 40G PCS core supports RS FEC described in IEEE 802.3 Clause 74 with independent error detection and error correction. The core supports the following features:

It implements 64b/66b encoding/decoding.

The core supports 40G scrambling/descrambling of polynomial $1 + x^{39} + x^{58}$

The core implements multi-Lane Distribution (MLD) across 4 Virtual Lanes (VLs).

Features

Full 40G MAC and PCS Core

- 40G MAC and 40G PCS Modules
- 40G RS FEC support with independent error bit detection and error bit correction
- 32 bit CRC generation on TX and 32 bit CRC check on RX
- Zero bytes padding for 64 bytes packets
- Pause Frame processing for flow control
- PCS gearbox on TX and RX
- 64b/66b encoding and decoding
- 40G scrambling and descrambling
- Multi-Lane Distribution over 4 Virtual Lanes.
- AM insertion and deletion on TX and RX.
- 64 bit block synchronization and Alignment Marker Lock algorithm support
- Multi-lane skew removal algorithm and virtual lane reordering
- BIP-8 generation/insertion on TX and BIP-8 check/removal on RX per virtual lanes.
- Link signaling protocol support.
- Bit Error Rate (BER) monitor support.
- Run time reset of clock domains and components.
- Configuration/Control/Status/States support.
- Separate clock domains for packet processing and control interfaces.
- 801.1Q tagging for VLAN
- MDIO module and External MDIO access via AXI4-Lite bus

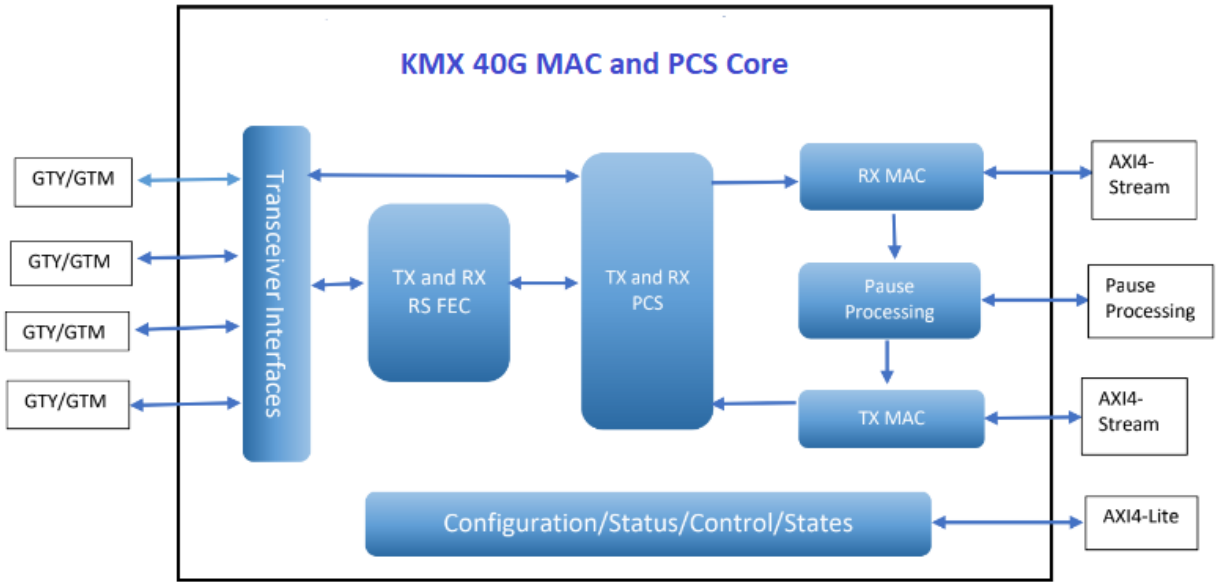

Figure 1 KMX 40G MAC/PCS Core Architecture

It implements periodic insertion of Alignment Marker (AM) on TX and deletion on RX. It supports PCS gearbox on TX and RX.

The 66-bit block synchronization and Alignment Marker Lock algorithm on RX are implemented.

It supports deskew algorithm.

The core implements lane reordering. It supports gearbox on both TX and RX

The BIP-8 generation and insertion on TX; BIP-8 checking on RX per virtual lane are supported.

It implements Bit Error Rate (BER) for monitoring excessive error ratio

The transceiver interface loopback for debug purpose is implemented, which at the transceiver interface, the data flow on transmit path is redirected to receive path and no data is forwarded to transceiver TX interface.

The core supports link signaling protocol.

Applications

The core is widely used in applications where ultra-low, deterministic latency and high performance of throughput are required, such as video, image and audio streaming over Ethernet, IP cameras VOIP and smart phones, high frequency trading system, high-speed communication data centers, device monitoring and control over IP networks. It works as a key component in network architecture.

Implementation Results

The 40G MAC and PCS Core has been evaluated on Xilinx platforms. The core is highly pipelined and optimized to achieve ultra-low latency and high performance. The following list the core sample resource utilization on Xilinx Kintex UltraScale+ device FPGA board KCU116.

Mode	LUT	LUTRAM	FF
No RS FEC	16432	1206	14724
RS FEC with error detect and no correct	21240	1614	19680
RS FEC with error detect and correct	30326	2102	26242

Support

The core as delivered are warranted against defects and any update of the core is made available for the customer with a valid KMX license. Free technical support is provided 7 days a week; 24 hours a day for these customers.

Deliverables

The core in netlist format included, the delivery package contains everything required for successful integration, including VHDL source code of reference design and test bench; verification scripts; constrain files; synthesis scripts; and related documentations. The VHDL source code of companion cores of MDIO module, serial debug command module with auto-configuration are shipped with the core delivery package to help customers for easy and efficient integration.

Contact

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