KMX EMBEDDED CORE 100G MAC and PCS Core

KMX 100G MAC and PCS core, which consists of media access control (MAC) module, physical coding sublayer (PCS) module and physical medium attachment (PMA) module, is compliant with the IEEE 802.3ba-2010 standard. The core implements RS FEC as defined in IEEE 802.3bj Clause 91 with independent bit error detection and bit error correction.

KMX 100G MAC module connects to user logic via AXI4-Stream interface of 320 bits at 312.5MHZ and to 100G PCS core via CGMII interface of 320 bits at 312.5 MHZ. It connects to user logic via AXI4-Lite interface.

The MAC core accepts packets from user logic and generates new format packets by adding Preamble/SFD; padding zero bytes for short packets to 64 bytes; generating 32 CRC and padding it. It receives packets from 100G PCS and generates new format packets by removing Preamble/SFD and 32 bit CRC after CRC checking.

It supports Pause Frame processing for flow control and implements Deficit Idle Count algorithm to ensure maximum possible throughput at the transmit interface.

The core implements internal CGMII loopback for debug purpose, where at the CGMII interface, the data flow on TX path is redirected to RX path and no data forwarded to transceiver TX interface.

It implements configuration, control, status, statistical information collection and it supports VLAN tagged frame defined IEEE 802.1Q.

KMX 100G PCS module connects to 100G MAC module via CGMII of 320 bits at 312.5MHZ and connects to transceiver interface at 320bits at 322.265625MHZ. The PCS core is compliant with IEEE 802.3ba specifications. The core supports RS FEC defined in IEEE 802.3bj. The core supports the following features:

It implements 64b/66b encoding/decoding.

The core supports 100G scrambling/descrambling of polynomial $1 + x^{39} + x^{58}$

It implements multi-Lane Distribution (MLD) across 20 Virtual Lanes (VLs)

Features

Full KMX MAC and PCS Core

- 100G MAC and 100G PCS Modules
- 100G RS FEC support with independent error bit detection and error bit correction
- 32 bit CRC generation on TX and 32 bit CRC check on RX
- Zero bytes padding for 64 bytes packets
- Pause Frame processing for flow control
- PCS gearbox on TX and RX.
- 64b/66b encoding and decoding
- 100G scrambling and descrambling
- Multi-Lane Distribution over 20 Virtual Lanes.
- AM insertion on TX and AM deletion on RX.
- 64 bit block synchronization algorithm and Alignment Marker Lock algorithm.
- Multi-Lane skew removal algorithm and virtual lane reordering
- BIP-8 generation, insertion on TX and BIP-8 check on RX on each of 20 virtual lanes.
- Link signaling protocol support.
- Bit Error Rate (BER) monitor support.
- Run time reset of clock domains and components.
- Configuration/Control/Status/States support.
- Separate clock domains for packet processing and control interfaces.
- 801.1Q tagging for VLAN
- MDIO module and External MDIO access via AXI4-Lite bus.

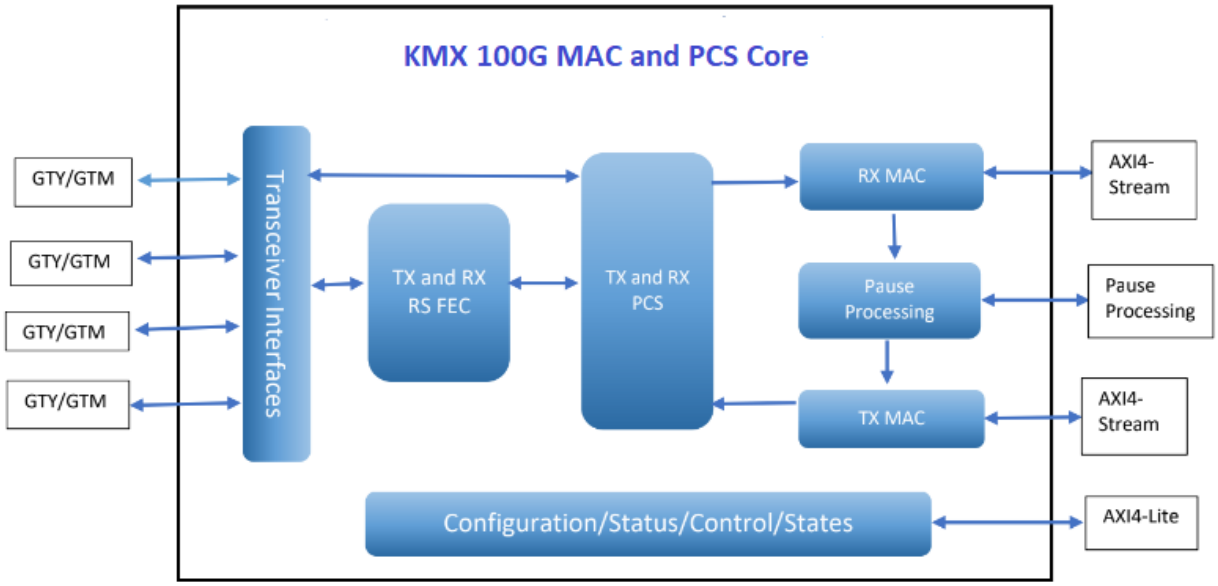

Figure 1 KMX 100G MAC/PCS Core Architecture

The core implements periodic insertion of Alignment Marker (AM) on TX and deletion on RX. It supports gearbox on RX and TX.

The 66-bit block synchronization and Alignment Marker Lock algorithm on RX are implemented.

It supports skew compensation logic in order to realign all the virtual lanes and reassemble an aggregate 100G stream (with all 20 64b/66b blocks in the correct order)

It implements lane reordering to support reception of any virtual lane (VL) on any physical lane (PL)

The BIP-8 generation and insertion on TX and BIP-8 checking on RX on all 20 Virtual Lanes are implemented.

It implements Bit Error Rate (BER) for monitoring excessive error ratio. In addition, the core implements various status and statistical information defined in the IEEE 802.3ba such as block synchronization status, AM lock status, multilane deskew, lane reordering status and BIP-8 error counters of 20 virtual lanes.

The core supports transceiver interface loopback for debug purpose where at the transceiver interface, the data flow on transmit path is redirected to the receive path and no data is forwarded to transceiver TX interface.

It implements link signaling protocol and Gearbox on both RX and TX.

Applications

The core is widely used in applications where ultra-low, deterministic latency and high performance of throughput are required, such as video, image and audio streaming over Ethernet, IP cameras VOIP and smart phones, high frequency trading system, high-speed communication data centers, device monitoring and control over IP networks. It works as a key component in network architecture.

Implementation Results

The 100G MAC and PCS Core has been evaluated on Xilinx platform. The core is highly pipelined and optimized to achieve ultra-low latency and high performance. The following list the core sample resource utilization on Xilinx Kintex UltraScale+ device FPGA board KCU116.

Mode	LUT	LUTRAM	FF
Without RS FEC	42802	2034	2308
RS FEC with error detect and correct	88872	4024	46854
RS FEC with error detect and no correct	56772	3012	31256

Support

The core as delivered are warranted against defects and any update of the core is made available for the customers with a valid KMX license. Technical support is free and provided 7 days a week; 24 hours a day to these customers.

Deliverables

The core in netlist format included, the delivery package contains everything required for successful integration, including VHDL source code of reference design and test bench; verification scripts; constrain files; synthesis scripts and related documents. The VHDL source code of companion cores of MDIO module, serial debug command module with auto-configuration is shipped with the core delivery package to help customers for easy and efficient integration.

Contact

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