AN and LT Core

KMX AN and LT core consists of Auto-Negotiation module and Link-Training module, which aims to build a reliable communication with remote link partner and to improve link quality for BER of 10^{-12}. The Auto-Negotiation and Link-Training conform to clause 72 and clause 73 in 802.3ap-2007 (IEEE Backplane Ethernet Standard).

KMX Auto-Negotiation consists of the following components: AutoNeg RX; AutoNeg TX; AutoNeg Page Generator; AutoNeg Arbitrator; AutoNeg Page Analyzer; DME Decoder; AutoNeg Control as indicated in Figure 1. These sub-modules are described in details in the following:

AutoNeg RX reads 64 bit data from transceiver RX interface, after lane 0 RX is locked, and reverses its bit order, pass it to DME Decoder.

AutoNeg TX transmits the encoded negotiation page to the transceiver TX interface.

AutoNeg Page Generator generates auto-negotiation page based on the information from AutoNeg Arbitrator, pass the page to DME Encoder.

AutoNeg Arbitrator implements the auto-negotiation arbitration defined in IEEE802.3ap-2007.

AutoNeg Page Analyzer tracks the received negotiation pages, handle INITIALIZE, PRESET, ACK and NEXT pages defined in IEEE802.3ap-2007, forwards the page information to AutoNeg Arbitrator.

DME Decoder decodes the received data from auto-negotiation pages and passes them to AutoNeg Page Analyzer.

AutoNeg Control connects to the user logic and work with AutoNeg Arbitrator to control the Auto-Negotiation process. It determines when to start auto-negotiation and when to end it.

When Auto-negotiation completes successfully, the core has enough information about the remote link partner to establish a communication.

Features

Full AN and LT Core

- KMX Auto-Negotiation Module and KNX Link-Training Module
- AutoNeg RX
- AutoNeg TX
- AutoNeg Page Generator
- AutoNeg Arbitrator
- AutoNeg Page Analyzer
- DME Decoder
- AutoNeg Control
- Training Frame RX
- Training Frame Lock
- LT DME Decoder
- Training Pattern Checker
- LT DME Encoder
- Training Pattern Generator
- Training Frame TX
- Training Engine
- Coefficient Update
- Link Training
- MDIO module and External MDIO access via AXI4-Lite bus

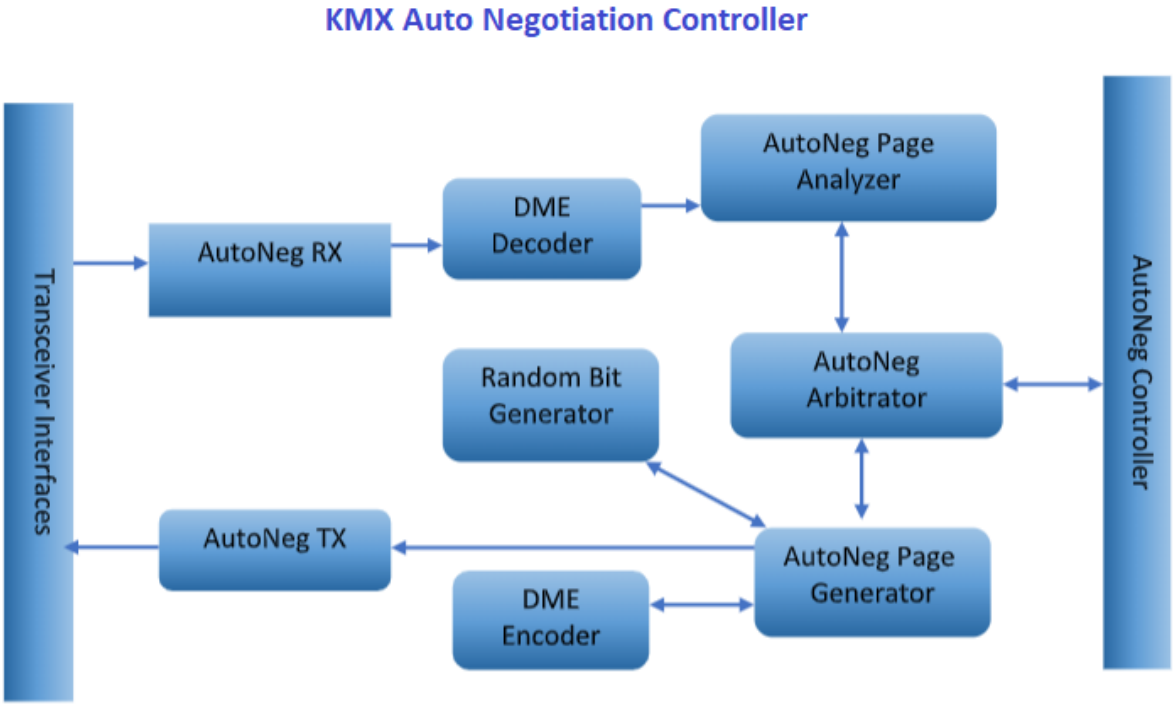

Figure 1 KMX AN Module Architecture

KMX Link-training module conforms to clause 72 in IEEE802.3ap-2007. It consists of the following components: Training Frame RX; Training Frame Lock; DME Decoder; DME Encoder; Training Pattern Checker; Training Pattern Generator; Coefficient Update; Link Training; Training Frame TX and Training Engine as indicated in Figure 2. These sub-modules are described in details in the following:

Training Frame RX checks if the lane 0 RX is locked (the RX output is valid) and when it is locked, reads the data from transceiver RX interface and reverses the order of 64 bit, passes the data to the Training Frame Lock module.

Training Frame Lock implements Training Frame Lock algorithm defined in IEEE802.3ap-2007. When Training Frame is locked, it passes the received data from transceiver RX interface to the DME Decoder and the Training Pattern Checker.

DME Decoder decodes the received training frames for the control channel message when training frame lock is achieved.

Training Pattern Checker checks the training pattern bit stream received from the link partner and passes the results to Link Training module.

DME Encoder generates control channel in DME format defined in IEEE802.3ap-2007 and passes the encoded control channel bit stream to Training Frame TX.

Training Pattern Generator generates the training pattern bit stream from polynomial x9 + x6 + 1 with seed configured by user logic and passes them to Training Frame TX.

Training Frame TX generates training frames and writes them to transceiver TX interfaces.

Training Engine implements the Training State defined in IEEE802.3ap-2007.

Coefficient Update configures the RX equalizer of transceiver with coefficient update value from Training Engine. This module is transceiver dependent. In Xilinx FPGA devices, It uses the DRP (Dynamic Reconfiguration Port) to update link coefficients for better RX equalizer. The coefficient initial value is read from transceiver interfaces.

Link Training controls Link Training process and determines when it starts and when it ends.

When link training process completes, the link has better quality and reliability.

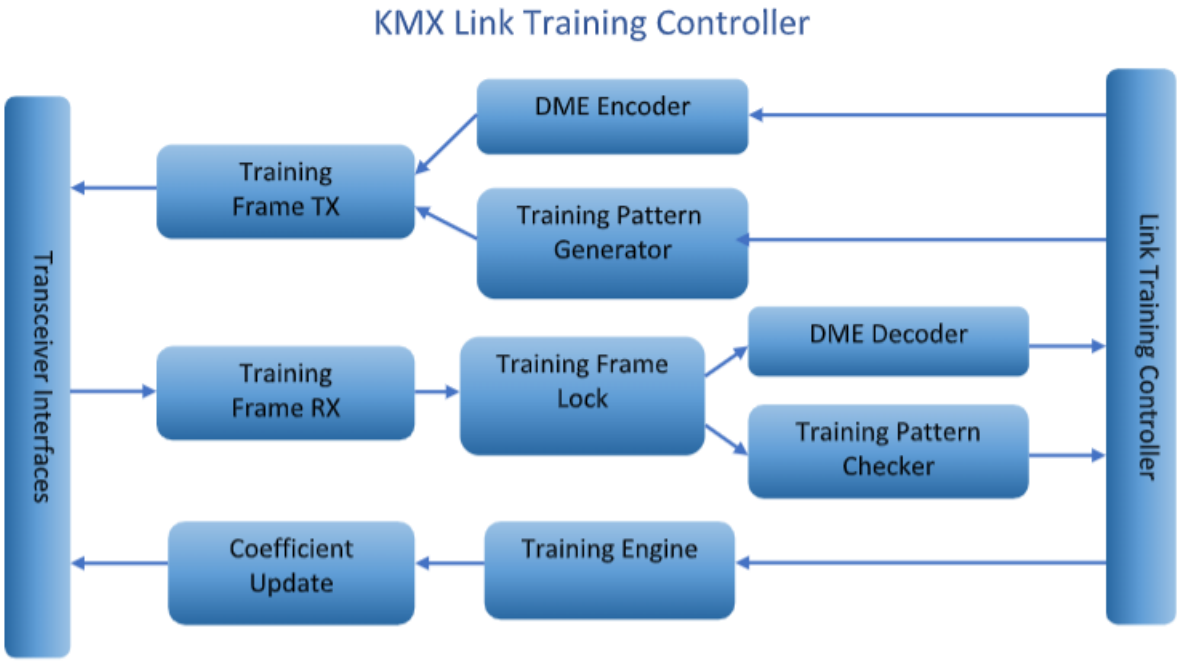

Figure 2 KMX LT Module Architecture

Applications

The core is widely used in applications where ultra-low, deterministic latency and high performance of throughput are required, such as video, image and audio streaming over Ethernet, IP cameras VOIP and smart phones, high frequency trading system, high-speed communication data centers, device monitoring and control over IP networks. It works as a key component in network architecture.

Implementation Results

The KMX AN and LT core has been evaluated on Xilinx platform. The core is highly pipelined and optimized to achieve ultra-low latency and high performance. The following list the core sample resource utilization on Xilinx Kintex UltraScale+ device FPGA board KCU116.

LUT	LUTRAM	FF
3599	51	6122

Support

The core as delivered are warranted against defects and any update of the core is made available for the customers with a valid KMX license. Free technical support is provided 7 days a week; 24 hours a day to these customers.

Deliverables

The core in netlist format included, the delivery package contains everything required for successful integration, including VHDL source code of reference design and test bench; verification scripts; constrain file; synthesis scripts and the related documentations. The VHDL source code of companion cores of MDIO module, serial debug command module with system auto-configuration is shipped with the delivery package to help customers for easy and efficient integration.

Contact

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